RECEIVED
CENTRAL FAX CENTER
APR 2 3 2007

REMARKS

Reconsideration of the above referenced application in view of the following remarks is requested. Claims 1, 11, 14, 18, 21, 24, 28, and 31 have been amended. Claims 2 and 32 were previously cancelled. Existing claims 1, 3-31, and 33 (as amended) remain in the application.

ARGUMENT

Claim Rejections – 35 USC § 112

Claims 11, 14, 18, 21, 24, and 28 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

Claims 11, 13, 18, 21, 24, and 28 have been amended and the term "inner relationship" has been deleted. As a result, Applicant submits that these claims (as currently amended) are enabled by the description.

Claim Rejections – 35 USC § 103

Claims 1 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (6,629,268) (hereinafter Arimilli_1) in view of WO 00/52582 (hereinafter WO reference).

Claims 2-10 and 32-33 are rejected under 35 U.S. C. 103(a) as being unpatentable over Arimilli_1 in view of the WO reference and further in view of Arimilli (2002/0129211) (hereinafter Arimilli_2).

In the Examiner's response to Applicant's argument filed on November 30, 2006, the Examiner stated that the feature "two cache coherency states associated with one cache line") is not recited in the rejected claims (see page 6 of the OA). In response, Applicant has amended independent claims 1 and 31 to expressly recite this feature. Applicant submits that the combination of Arimilli_1, Arimilli_2, and the WO reference does not teach or suggest this feature. Thus, claims 1 and 31, as amended, are patentable of the combination of the cited references. Accordingly, all of the claims that depend therefrom (i.e., claims 3-10, and claim 33, respectfully) are also patentable over the combination of the cited references.

Claims 11-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli_2 in view of the WO reference.

Regarding independent claims 11, 14, 18, 21, 24, and 28, the Examiner asserted that Fig. 3, page 7; line 27 to page 8, line 13; and page 15, lines 1-19 of the WO reference discloses the limitation of transitioning a first cache coherency state to a joint cache coherency state including a first cache coherency state for outer interfaces and a third cache coherency state for inner interfaces. Applicant respectfully disagrees. Fig. 2 of the WO references shows a state transition diagram based on MESI protocol and Fig. 3 of the WO reference shows the state transition diagram based on the MESI protocol with expanded coherency states (i.e., joint states). There is no showing by the cited portions of the WO reference of transitions from a single MESI coherency state (e.g., M or E) to a joint coherency state (e.g., MI), as recited by the claimed limitation.

In response to the above argument in the Advisory Action of October 16, 2006, the Examiner stated that the feature—transitions from a single cache coherency state (i.e., a single MESI state) to a joint coherency state (e.g., MI)—is not recited in the rejected claims. To make this feature more explicit in claims 11, 14, 18, 21, 24, and 28, these claims have been amended to make it clear that the first cache coherency state is a single cache coherency state. By adding this limitation to claims 11, 14, 18, 21, 24, and 28, the limitation of transitioning the first cache coherency state to a joint cache coherency state, originally recited in these claims, is now very clear that it means transitions from a single state to a joint state.

In the Office Action of December 22, 2006, the Examiner asserted, "The WO reference clearly shows single TLC state (e.g., I, S, E, M) and single SLC state (e.g., I, S, E, M) transitioning to joint coherency state (e.g., SI, ES, EM, MI, MI, MS...)." Applicant respectfully disagrees. The Examiner did not specifically point out which portion of the WO reference supports the Examiner's assertion. Probably the Examiner made this assertion based on FIG. 4. A review of the description of FIG. 4 on page 14 (lower portion) through page 16 (upper portion) reveals that FIG. 4 simply compares single state coherency protocol and the expended states coherency protocol to show advantages of the latter. It does not show, expressly or implicitly, transitions from a single coherency state to a joint coherency state. As Applicant pointed out above, the cited portion of the WO reference (i.e., FIG. 3, page 7, line 27 to page 8, line 13; page 15, lines 1-19) does not teach or suggest this limitation at all. Thus, the Applicant respectfully requests that the Examiner particularly point out which portion of the WO reference teaches or suggests this limitation. Without any support from the cited

reference for the Examiner's assertion, Applicant submits that the WO reference does not teach or suggest this limitation at issue.

For the foregoing reasons, the combination of Arimilli_2 and the WO reference does not teach or suggest all of the limitations recited in independent claims 11, 14, 18, 21, 24, and 28, as amended. Thus, these claims are patentable over Arimilli_2 in view of the WO reference. Accordingly, all of the claims that depend therefrom are also patentable over Arimilli_2 in view of the WO reference. Applicant hereby respectfully requests that the Examiner withdraw the 35 USC § 103 rejections of claims 11-30.

CONCLUSION

Based on the foregoing, it is submitted that that all active claims are presently in condition for allowance, and their passage to issuance is respectfully solicited. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (503) 264-1700. Entry of this amendment is respectfully requested.

Respectfully submitted,

Date: April 23, 2007

/Guoujun Zhou/
Guojun Zhou
Registration No. 56,478
INTEL CORPORATION
MS JF3-147
2111 NE 25th Ave.
Hillsboro, OR. 97124